

SM2260 L06B F/W Release Note

FW Package	MP Tool Version	ISP Version	Note
C2.3.7	V3.2.13	C2.3.7	<ul style="list-style-type: none"> ● FW Changes <ul style="list-style-type: none"> - Adjust TrainAdj max error bit in MPISP. - Enhance PCIe error handling flow. - Enable ATA security to support password and authentication. - Enable Flash I/O 1.2V and 1.8V support (configured by MP Tool) ● MP Tool Changes <ul style="list-style-type: none"> - Add TrainAdj configuration, for user to input ECC threshold and bypass mode (don't care TrainAdj result) - Enable option of DRAM trained window check - Add display of error count info, RDT setting info, and bad block table in "RDT Result" page.
C2.2.3	V3.2.5	C2.2.3	<ul style="list-style-type: none"> ● Enable Samsung DRAM settings for 128/256/512/1024GB SSD configurations. ● Limit the number of active program/erase dies. ● Fine tune thermal throttling settings to limit PS1 performance degradation within 20% (compared to PS0). ● Use 4B Read in Get Feature to avoid NAND compatibility issue (some previous version not allowing 1B Read). ● Separate the PFail Switch from VDT120. ● Enhance RDT features in MP Tool.
C2.1.9	V3.2.3	C2.1.9	<ul style="list-style-type: none"> ● Support 2LUNs/CE for 1TB drive configuration ● Enable MIRA DRAM setting. ● Support to erase previous INFO blocks. ● MP V3.2.3 enable the following features <ul style="list-style-type: none"> - Add RDT Kick Off Command after load RDT FW - Update SMI driver to "WinDrv2260_142000_20161117.zip" - Support 8P Tester (8P HW Tester is not released yet, available in Jan.'17) - Add Date (YY/MM/DD) Mask of serial number - Add "Erase Previous Info Blocks" option in Pretest setting (("EraseInfoBlk" of "OPTION" in System.ini)) - Add DRAM vendor MIRA - Add to save BarCode list to \\LogFile\BarCode.txt
C2.1.6	V3.2.0	C2.1.6	<ul style="list-style-type: none"> ● Rollback to use Set Feature to switch between SLC and TLC modes since some NAND parts may not be capable of 0xDA/0xDF commands. ● Add 2-steps PS4 feature. The number of PS3 stay time in LightSwitch is used to toggle this feature (e.g. number != 0 to enable; number = 0 to disable). ● Update MPTool to support 2x 4-port tester (cascaded as 8-port tester). ● Enable NAND ODT features. ● Disable L0s support in ASPM by default (configurable in MPTool). ● Bug fixes for 2TB drive and enhance error recovery statistics for 2TB configuration. ● Update SMI drive to "WinDrv2260_141800_20161024.zip". ● Update EZTool to "EzTools_2260_Micron_P1114A_V1.2.12".

C2.1.3	V3.1.3	C2.1.3	<ul style="list-style-type: none"> ● Snap Read enablement, code optimization, and Flash command process flow optimization for random performance enhancement (mainly for 1024GB). ● Enable 2TB support. ● Enable P-Fail feature (needs PCB power circuit to support). ● Enhance sequential write performance (especially 128/256GB) by changing ultra-block RAID to super-block, cache program, and DA/DF commands. Due to higher RAID overhead, the “binary capacity” would be not achievable. ● Add features of MPTool, including new logs by date and bar code scan. ● Add configurability of APST in MPTool, and default is APST disabled.
C2.0.8	V3.1.2	C2.0.8	<ul style="list-style-type: none"> ● Remove IEEE in Identify Controller and EUI64 in Identify Namespace. ● Update NGUID for Win10 compatibility issue. ● Shrink write cache size to 3MB. ● Disable setup PERST GPIO20 interrupt. ● Upgrade MP Tool to V3.1.2 and driver, “WinDrv2260_141700_20160921.zip”.
C2.0.5	V3.1.0	C2.0.5	<ul style="list-style-type: none"> ● Enable “Whole Drive SLC Mode”, which is configurable via MP Tool. ● Bug fixes for PCIe 4-port Tester MFG SW. ● Update MP Tool driver, “WinDrv2260_9941501_20160913.zip”.
C2.0.0	V3.0.1	C2.2.0	<ul style="list-style-type: none"> ● Enable Intel L06B. ● Update DRAM parameters. ● Enable multi-port initialization on 4-port Tester.
C1.0.5	V2.2.2	C1.0.5	<ul style="list-style-type: none"> ● Initial FW release, including MPTool and EZTool. ● Support Micron L06B.

Note:

1. F/W and ISP update is recommended.
2. History # is denoted by “Version-Date”.

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